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DORSEY & WHITNEY LLP
INTELLECTUAL PROPERTY DEPARTMENT
SUITE 3400
1420 FIFTH AVENUE
SEATTLE, WA 98101

EXAMINER	
LE, DINH THANH	

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte GARY M. JOHNSON

Appeal 2009-1023
Application 10/733,605
Technology Center 2800

Decided[1]: May 11, 2009

Before JOSEPH F. RUGGIERO, MAHSHID D. SAADAT, and ROBERT E. NAPPI, *Administrative Patent Judges*.

SAADAT, *Administrative Patent Judge*.

DECISION ON APPEAL

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[1] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, begins to run from the decided date shown on this page of the decision. The time period does not run from the Mail Date (paper delivery) or Notification Date (electronic delivery).

Appellant appeals under 35 U.S.C. § 134(a) from a Final Rejection of claims 1-4, 9, 10, 25-28, 33-38, 43, and 44. Claims 11-24 and 45-49 have been canceled and claims 5-8, 29-32, and 39-42 have been objected to as containing allowable subject matter, but being dependent upon rejected base claims. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

STATEMENT OF CASE

Appellant's invention relates to a delay lock loop that provides an output signal based upon a phase difference between a reference signal and a feedback signal (Spec. 5:1-6). Claim 1 is illustrative of the claimed invention and reads as follows:

1. A device, comprising:

delay lock loop to provide an output signal based upon a phase difference between a reference signal and a feedback signal, said delay lock loop comprising a delay circuit for activating a transistive capacitive delay.

The prior art applied in rejecting the claims on appeal is:

Johnson	US 5,101,117	Mar. 31, 1992
Baker	US 6,445,231 B1	Sep. 3, 2002
Lee	US 6,483,359 B2	Nov. 19, 2002

Claims 1-4, 9, 10, 35-38, 43, and 44 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee in view of Johnson.

Claims 1-4, 9, 10, 25-28, 33-38, 43, and 44 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Baker in view of Lee and Johnson.

We refer to the Briefs (Appeal Brief filed Jul. 16, 2007 and Reply Brief filed Dec. 26, 2007) and the Answer (mailed Oct. 18, 2007) for their

respective details. Only those arguments actually made by Appellant have been considered in this decision. Arguments which Appellant did not make in the Briefs have not been considered and are deemed waived. *See* 37 C.F.R. § 41.37(c)(1)(vii).

ISSUE

The Examiner relies on Lee for disclosing the delay lock loop and its delay circuit of claim 1 except for the claimed delay circuit activating a transistive capacitive delay, for which the Examiner relies on Johnson (Ans. 3-4). In particular, the Examiner points to Figure 1 of Johnson where switches 71*a*-71*l* activate transistive capacitors 72*a*-72*l* (Ans. 4) and states that those capacitors are similar to the claimed delay lock loop comprising a delay circuit that activates a transistive capacitive delay.

Appellant does not dispute the teachings of Lee with respect to the claimed delay lock loop and the generated output signal and merely challenges the teachings of Lee or Johnson with respect to the claimed transistive capacitive elements (App. Br. 4-10). Appellant further contends that one of ordinary skill in the art would not have combined the teachings of Lee with those of Johnson (App. Br. 10-11). Appellant specifically argues that the combination of the references does not teach all the claimed features since transistors 72*a*-72*l*, shown in Figure 4 of Johnson, are passive capacitors (App. Br. 8-9).

Therefore, the issue before us is whether under 35 U.S.C. § 103(a), the ordinarily skilled artisan would have found it obvious to combine Lee and Johnson to render the claimed invention unpatentable by teaching "a transistive capacitive delay" for use in a delay lock loop.

FINDINGS OF FACT

1. Lee relates to a delay lock loop (DLL) including an external clock signal as the reference signal received at clock buffer 300, a delay line 340 and a feedback signal generated by delay monitor 310, for generating an output signal DLL_CLK (Abstract; col. 2, ll. 54-65; fig. 3).

2. As shown in Figure 4, Lee uses capacitors C1, C2, C3 in serial connection with switching capacitors 345, 346, and 347 as the delay line 340 (col. 4, ll. 15-27).

3. Johnson discloses a variable delay line phase locked loop technique for delaying a clock signal (col. 1, ll. 53-57).

4. The delay line disclosed by Johnson, as shown in Figure 4, includes a series of drivers 70*a*-70*l*, control transistors 71*a*-71*l*, and capacitors 72*a*-72*l* (col. 4, ll. 39-43).

5. Johnson discloses that drivers 70*a*-70*l* control the switching of transistors 71*a*-71*l* in order to couple the capacitors 72*a*-72*l* directly to the output terminal (col. 4, ll. 47-54).

6. Baker relates to a dual-loop digital delay locked loop (DLL) including a coarse loop and a fine loop for providing a full range of adjustments (col. 1, ll. 54-67; figs. 1, 2A, and 3A).

PRINCIPLES OF LAW

The test for obviousness is what the combined teachings of the references would have suggested to one of ordinary skill in the art. *See In re Kahn*, 441 F.3d 977, 987-88 (Fed. Cir. 2006); *In re Young*, 927 F.2d 588, 591 (Fed. Cir. 1991); *In re Keller*, 642 F.2d 413, 425 (CCPA 1981).

> Section 103 forbids issuance of a patent when "the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains."

KSR Int'l Co. v. Teleflex Inc., 550 U.S. 398 406 (2007).

"'The combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results.'" *Leapfrog Enters., Inc. v. Fisher-Price, Inc.*, 485 F.3d 1157, 1161 (Fed. Cir. 2007) (quoting *KSR*, 550 U.S. at 416). "One of the ways in which a patent's subject matter can be proved obvious is by noting that there existed at the time of invention a known problem for which there was an obvious solution encompassed by the patent's claims." *KSR*, 550 U.S. at 419-20.

ANALYSIS

I. Rejection of claims 1-4, 9, 10, 35-38, 43, and 44 under 35 U.S.C. § 103(a) over Lee and Johnson

We agree with the Examiner's line of reasoning and find that Johnson does teach using a delay circuit for activating a transistive capacitive delay. As pointed out by the Examiner (Ans. 6), the claims do not specifically recite "active capacitors" or "passive capacitors" in describing the claimed capacitive delay. The Examiner appropriately relies (Ans. 6) on the only example of a transistive capacitor provided by Appellant shown as capacitors 540 and 550 in Figure 5 of the instant application to conclude that a transistive capacitor refers to "a transistor being connected to function as a capacitor" (*id.*).

This interpretation is reasonable and consistent with Appellant's disclosure describing that each of the transistor sets 540 or 550 "takes on the role of a capacitor" (Spec. 17:19-24) to provide a relatively constant capacitance (Spec. 19:3-15). Therefore, contrary to Appellant's argument that Johnson labels devices 72*a*-72*l* as merely "load capacitors" (Reply Br. 3), we find that transistors 72*a*-72*l* of Johnson function as capacitors that are activated by drivers 70*a*-70*l* and controlled by transistors 71*a*-71*l* (FF 3-5). In other words, similar to the transistors shown in Appellant's Figure 5, each of transistors 72*a*-72*l* takes on the role of a capacitor.

We also disagree with Appellant's argument against the desirability of combining the references and whether the references are analogous (App. Br. 10-11; Reply Br. 5-6). Lee provides for a delay lock loop for producing an output signal based on a phase difference between a reference signal and a feedback signal (FF 1), where the delay circuit includes a series of capacitors (FF 2). Johnson was relied on for specifically using transistive capacitors in a delay line phase locked loop (FF 3-5). Johnson further teaches that such transistive capacitive delay is activated by drivers 70*a*-70*l* (FF 5).

In that regard, using *KSR* and *Leapfrog* standards, the evidence provided by the Examiner supports a finding that combining the familiar transistive capacitors of Johnson with the delay lock loop of Lee is based on using an obvious solution to a known problem. Such combination would have been obvious to one of ordinary skill in the art since it also produces predictable results with respect to replacing the capacitive elements in the delay line of Lee with similar capacitors such as the transistive capacitors 72*a*-72*l* of Johnson. Thus, we sustain the 35 U.S.C. § 103(a) rejection of

claims 1 and 35, as well as claims 2-4, 9, 10, 36-38, 43, and 44 argued together with their base claims (App. Br. 11), over the teachings of Lee and Johnson.

II. Rejection of claims 1-4, 9, 10, 25-28, 33-38, 43, and 44 under 35 U.S.C. § 103(a) over Baker, Lee, and Johnson

Appellant argues that the combination of the references is improper since Baker does not teach or disclose a delay circuit for activating a transistive capacitive delay, nor is there a motivation to combine the DLL loop of Lee and Johnson with Baker (App. Br. 11-12; Reply Br. 5-6). The Examiner responds by relying on the arguments made with respect to claims 1 and 35, addressed *supra*, regarding the use of the transistive capacitors of Johnson (Ans. 7-8). The Examiner further points to the delay lock loop of Baker shown in Figures 1, 2A, and 3A and asserts that such DLL circuit would have benefited from using the transistive capacitors suggested collectively by Lee and Johnson (Ans. 10).

We agree with the Examiner and, for similar reasons discussed above with respect to claims 1 and 35, find the combination of the transistive capacitors used in a DLL loop of Lee and Johnson with Baker's DLL to be reasonable. We also note that Appellant's contention related to Baker's teaching of a DLL (App. Br. 12) is misplaced since Baker does indeed disclose a delay circuit (FF 6). Therefore, contrary to Appellant's argument (App. Br. 12; Reply Br. 5-6) and according to *Leapfrog*, using the transistive capacitors of Lee and Johnson in combination with the DLL circuit of Baker would constitute a combination of familiar transistive capacitive elements in a DLL circuit according to methods known to the skilled artisan with a

predictable result, which is likely to be obvious. Thus, we sustain the 35 U.S.C. § 103(a) rejection of claims 1, 25, and 35, as well as claims 2-4, 9, 10, 24, 26-28, 33, 34, 36-38, 43, and 44 argued together with their base claims (App. Br. 13), over the teachings of Baker, Lee, and Johnson.

CONCLUSION

In view of our analysis above, we do not find error in the Examiner's position with respect to the combination of the applied references. We find that the teachings of Lee and Johnson, as well as the teachings of Baker, Lee, and Johnson, when considered as a whole, support the Examiner's 35 U.S.C. § 103 ground of rejection by teaching "a transistive capacitive delay" for use in a delay lock loop. Thus, we sustain the 35 U.S.C. § 103(a) rejection of claims 1-4, 9, 10, 35-38, 43, and 44 over Lee in view of Johnson and of claims 1-4, 9, 10, 25-28, 33-38, 43, and 44 over Baker in view of Lee and Johnson.

ORDER

The decision of the Examiner rejecting claims 1-4, 9, 10, 25-28, 33-38, 43, and 44 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

gvw

DORSEY & WHITNEY LLP
INTELLECTUAL PROPERTY DEPARTMENT
SUITE 3400
1420 FIFTH AVENUE
SEATTLE, WA 98101